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61591 U.S. PTO
09/18/97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Docket No. **93-C-07C2**
Examiner: **T. Cunningham**
Art Unit: **2504**

REQUEST FOR FILE WRAPPER CONTINUING APPLICATION UNDER 37 CFR 1.62

Box: **FWC**
HONORABLE COMMISSIONER OF
PATENTS AND TRADEMARKS
WASHINGTON, D.C. 20231

SIR: This is a request for filing a _____ continuation-in-part __X____ continuation _____ divisional application under 37 CFR 1.62, of prior application serial no. 08/606,232 filed on February 23, 1996, entitled *DIRECT CURRENT SUM BANDGAP VOLTAGE COMPARATOR* by the following named inventor(s).

Full Name of Inventor:	William Carl Slemmer
Residence Address:	9114 Arborside Drive
City, County, State	Dallas, Dallas County, Texas 75423
Citizenship:	U.S.A.
Post Office Address:	Same as Residence

The above identified prior application in which no payment of the issue fee, abandonment of, or termination of proceedings has occurred, is hereby expressly abandoned as of the filing date of this new application. Please use all the contents of the prior application file wrapper, including the drawings, as the basic papers for the new application. (Note: 37 CFR 1.60 may be used for applications where the prior application is not to be abandoned.)

1._____Enter the amendment previously filed on * under 37 CFR 1.116 but unentered, in the prior application.

2._____X_____A preliminary amendment is enclosed.

3._____XX_____The filing fee is calculated on the basis of the claims existing in the prior application as amended at 1 and 2 above.

Basic Fee		$770.00
Extra Total Claims (____ x $22.00)	=	
Extra Independent Claims (____ x $80.00)	=	
Total Filing Fee:	=	$770.00

Certificate of Mailing Under 37 C.F.R. § 1.18(a)

I certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner of Patents, Washington, D.C. 20231 on September 15, 1997.

by Carolyn Wright
Carolyn Wright

4. XX The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required, or credit any overpayment to Account No. 06-0580.

5. XX A check in the amount of $770.00 is enclosed.

6. ____ A new oath or declaration is included since this application is a continuation-in-part which discloses and claims additional matter.

7. XX Amend the specification by inserting before the first line of the following sentence:

This is a ____ Continuation-in-part, XX continuation, ____ Division, of application serial no. 08/606,233, filed February 23, 1996.

8. ____ A verified statement claiming small entity status is enclosed, (necessary even if a statement was filed in the prior application).

9. ____ Priority of application serial no. *, filed on *, in * is claimed under 35 U.S.C.119.

10. XX The prior application is assigned of record to SGS-Thomson Microelectronics, Inc.

11. XX The power of attorney in the prior application is to Richard Robinson, Reg. No. 28,109 and Lisa K. Jorgenson, Reg. No. 34,845.

12. XX Address all future communications to: Lisa K. Jorgenson, SGS-Thomson Microelectronics, Inc., 1310 Electronics Drive, M/S 2346, Carrollton, Texas 75006.

13. ____ Also enclosed: *

It is understood that secrecy under 35 U.S.C. 122 is hereby waived to the extent that if information or access is available to any one of the applications in the file wrapper of a 37 CFR 1.62 application, be it either this application or a prior application in the same file wrapper, the Patent and Trademark Office may provide similar information or access to all the other application in the same file wrapper.

9-15-97
(Date)

Harold E. Venglarik
(Signature)

Address of signature

Dan Venglarik
Felsman, Bradley,
Gunter & Dillon, LLP
2600 Continental Plaza
777 Main Street
Fort Worth, Texas 76102

____ Inventors(s)
____ Assignee of complete interest
____ Attorney or agent of record
_X_ Filed under Section 1.34(a)

1004KH-16316/47115.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
W. SLEMMER

Serial No. **08/606,233**

Filed: **FEBRUARY 23, 1996**

For: **DIRECT CURRENT SUM BANDGAP VOLTAGE COMPARATOR**

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§
§ Group Art Unit: **2504**
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§ Examiner: **Cunningham, T.**
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§ Attorney Dkt. No.: **93-C-07C1**
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Certificate of Mailing Under 37 C.F.R. § 1.8(a)
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By: Carolyn Wright
Carolyn Wright

TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Enclosed please find:

- Rule 1.62 Continuation Application;
- Preliminary Amendment;
- Petition for Extension of Time Within the Second Month;
- Amendment Under 37 C.F.R. § 1.116;
- Our checks for $770.00 for the filing fee and $390.00 for the extension fee; and
- Our return postcard which we would appreciate your date stamping and returning to us upon receipt.

DATE: 9-15-97

Respectfully submitted,

Dan Venglarik

Dan Venglarik
Reg. No. 39,409
FELSMAN, BRADLEY, GUNTER & DILLON, LLP
2600 Continental Plaza
777 Main Street
Fort Worth, TX 76102
(817) 332-8143

ATTORNEY FOR APPLICANT

1004KH-24316/47129.1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
W. SLEMMER

Serial No.

Filed: **HEREWITH**

For: **DIRECT CURRENT SUM BANDGAP VOLTAGE COMPARATOR**

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§ Group Art Unit:
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§ Examiner:
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§ Attorney Dkt. No.: **93-C-07C2**
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By: Carolyn Wright
Carolyn Wright

PRELIMINARY AMENDMENT

Box: FWC
Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination of the above-identified continuation application, please amend the application as follows. A check for the required fees is enclosed.

IN THE CLAIMS:

Please cancel claims 1, 4-14, 17-26 and 30.

Please amend the claims as follows:

27. (twice amended) A direct current sum bandgap voltage comparator comprising:

a power supply having a predetermined threshold voltage level which defines the minimum acceptable voltage level of the power supply;

a summing node;

a plurality of current sources connected to the summing node and directly connected to a power supply voltage, each current source further comprising at least one **field effect** transistor **and at least one bipolar junction transistor** and each current

source supplying a current to the summing node; and

an indicator circuit having an input connected to the summing node, wherein the indicator circuit is responsive to changes in the summing node voltage level and generates at an output a logical signal at one state when the summing node voltage level is greater than the predetermined threshold voltage level and generates the logical signal at the output at another state when the summing node voltage level is less than the predetermined threshold voltage level.

Please add the following new claims:

--31. A direct current sum bandgap voltage comparator comprising:

a summing node;

first and second current sources connected between the summing node and a lower power supply; and

third and fourth current sources connected between the summing node and an upper power supply,

wherein a voltage at the summing node equals a voltage of the upper power supply when a current from the first and second current sources to the summing node exceeds a current from the third and fourth current sources to the summing node, and

wherein the voltage at the summing node equals a voltage of the lower power supply when the current from the third and fourth current sources to the summing node exceeds the current from the first and second current sources to the summing node.

32. The direct current sum bandgap voltage comparator of claim 31, wherein the first current source further comprises:

a first field effect transistor connected between the lower power supply and the summing node;

a second field effect transistor connected at a source to the lower power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor;

a third field effect transistor connected at a source to the

lower power supply and connected at a gate to the gate of the first field effect transistor;

a fourth field effect transistors connected at a drain to the drain of the second field effect transistor;

a fifth field effect transistor connected at a drain to a drain of the third field effect transistor and to a gate of the fifth field effect transistor and connected at the gate to a gate of the fourth field effect transistor;

a first bipolar junction transistor connected at a base and a collector to the upper power supply;

a second bipolar junction transistor connected at a base and a collector to the upper power supply and connected at an emitter to a source of the fifth field effect transistor; and

a resistor connected to an emitter of the first bipolar junction transistor and to a source of the fourth field effect transistor.

33. The direct current sum bandgap voltage comparator of claim 32, wherein the first, second, and third field effect transistors are n-channel MOSFETs and the fourth and fifth field effect transistors are p-channel MOSFETs.

34. The direct current sum bandgap voltage comparator of claim 32, wherein the first field effect transistor is sized to generate a current of N times a current flowing through the second field effect transistor.

35. The direct current sum bandgap voltage comparator of claim 31, wherein the first current source further comprises:

a current mirror including a field effect transistor connected between the lower power supply and the summing node, wherein the field effect transistor is sized to generate a current of N times a current flowing through a portion of the current mirror.

36. The direct current sum bandgap voltage comparator of claim 31, wherein the second current source further comprises:

a first field effect transistor connected between the lower power supply and the summing node;

a second field effect transistor connected at a source to the lower power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor;

a third field effect transistor connected at a source to the lower power supply and connected at a gate to the gate of the first field effect transistor;

a fourth field effect transistor connected at a drain to the drain of the second field effect transistor;

a fifth field effect transistor connected at a drain to a drain of the third field effect transistor and to a gate of the fifth field effect transistor and connected at the gate to a gate of the fourth field effect transistor;

a bipolar junction transistor connected at a base and a collector to the upper power supply and at an emitter to the source of the fifth field effect transistor; and

a resistor connected between a source of the fourth field effect transistor and the upper power supply.

37. The direct current sum bandgap voltage comparator of claim 36, wherein the first, second, and third field effect transistors are n-channel MOSFETs and the fourth and fifth field effect transistors are p-channel MOSFETs.

38. The direct current sum bandgap voltage comparator of claim 31, wherein the third current source further comprises:

a first field effect transistor connected between the upper power supply and the summing node;

a second field effect transistor connected at a source to the upper power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor;

a third field effect transistor connected at a source to the lower power supply and connected at a drain to the drain of the second field effect transistor;

a fourth field effect transistor connected at a source to the lower power supply, at a gate to a gate of the third field effect transistor, and at a drain to the gate of the fourth field effect transistor;

a fifth field effect transistor connected at a source to the lower power supply;

a sixth field effect transistor connected at a drain to the drain of the fourth field effect transistor;

a seventh field effect transistor connected at a drain to a drain of the fifth field effect transistor and to a gate of the seventh field effect transistor and connected at the gate to a gate of the sixth field effect transistor;

an eighth field effect transistor connected at a drain and at a gate to a source of the seventh field effect transistor and at a source to the upper power supply; and

a resistor connected between a source of the sixth field effect transistor and the upper power supply.

39. The direct current sum bandgap voltage comparator of claim 38, wherein the first, second, sixth, seventh, and eighth field effect transistors are p-channel MOSFETs and the third, fourth and fifth field effect transistors are n-channel MOSFETs.

40. The direct current sum bandgap voltage comparator of claim 31, wherein the fourth current source further comprises:

a first field effect transistor connected between the upper power supply and the summing node;

a second field effect transistor connected at a source to the upper power supply and connected at a gate to a gate of the first field effect transistor and a drain of the second field effect transistor; and

a resistor connected between a drain of the second field effect transistor and the lower power supply.

41. The direct current sum bandgap voltage comparator of claim 40, wherein the first and second field effect transistors are p-channel MOSFETs.

42. The direct current sum bandgap voltage comparator of claim 31, further comprising:

a cascode stage connected to the summing node.

43. The direct current sum bandgap voltage comparator of claim 31, further comprising:

a clamping circuit connected to the summing node.

44. The direct current sum bandgap voltage comparator of claim 31, further comprising:

a plurality of inverters connected in series between the summing node and an output node.

45. The direct current sum bandgap voltage comparator of claim 31, further comprising:

a hysteresis circuit connected to the output node and to the fourth current source.--

REMARKS

Claims 27, 29, and 31-45 are pending in the present application. Claims 1, 4-14, 17-26, and 30 were canceled. Examination of the application is respectfully requested.

The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

Dan Venglarik
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& DILLON, LLP
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777 Main Street
Fort Worth, TX 76102
(817) 332-8143
ATTORNEY FOR APPLICANTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
W. SLEMMER

Serial No. **08/606,233**

Filed: **FEBRUARY 23, 1996**

For: **DIRECT CURRENT SUM BANDGAP VOLTAGE COMPARATOR**

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§ Group Art Unit: **2504**
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By: Carolyn Wright
Carolyn Wright

AMENDMENT UNDER 37 C.F.R. § 1.116

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

A two month extension of time is believed to be required. An appropriate petition and fee are enclosed. No additional fees are believed to be necessary; however, in the event that any additional fees are required for the prosecution of this application, please charge any necessary fees to Deposit Account No. 06-0580. No additional extension of time is believed to be necessary. If, however, an additional extension of time is needed, the extension is requested and please charge the fee for this extension to Deposit Account No. 06-0580.

In response to the Office Action dated January 15, 1997, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 27 and 29.

REMARKS

The application has been amended to cancel all claims not indicated to be allowable in the Office Action dated 01/15/97

(Paper No. 16).

It is respectfully urged that the subject application is now in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

Respectfully submitted,

Date: September 15, 1997

Dan Venglarik
Reg. No. 39,409

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